

## MSM6544

### 42-DOT LCD DRIVER

#### GENERAL DESCRIPTION

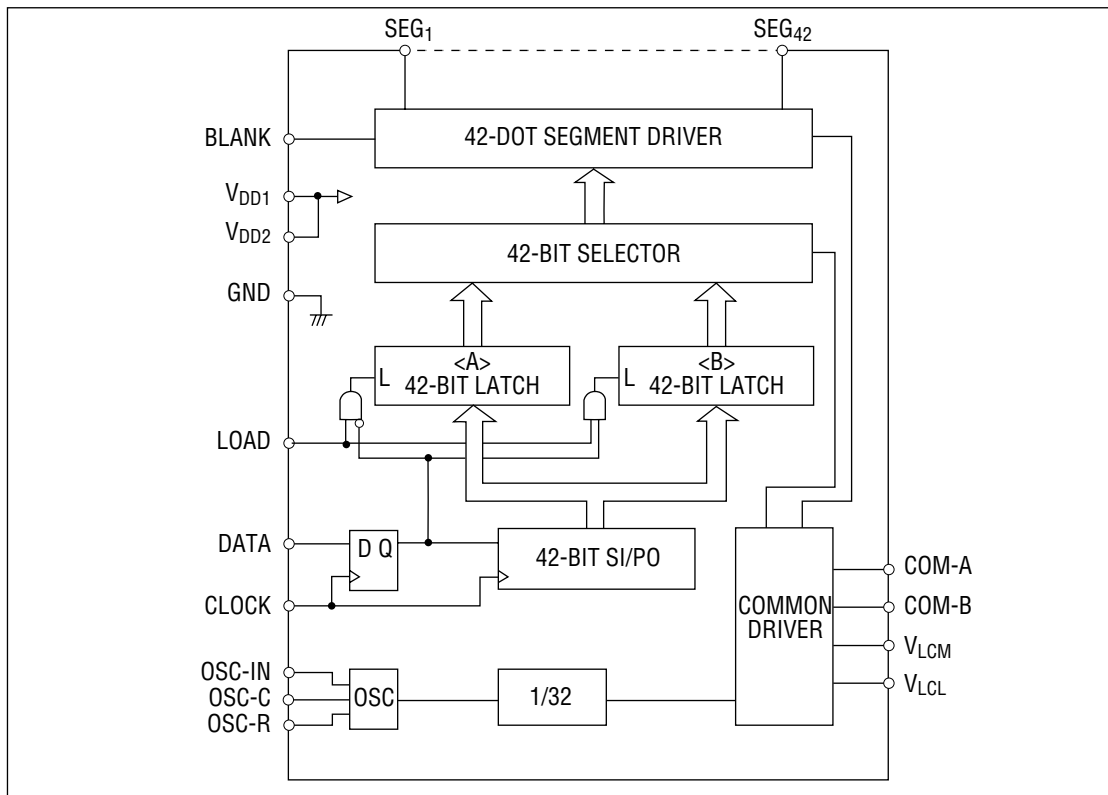
The MSM6544 is a 42-segment duplex driver which can drive the LCD panel up to a maximum of 84 segments.

Since the package is a 56-pin small QFP, an LCD module can be compactly configured. An internal RC oscillator is provided for ease of use.

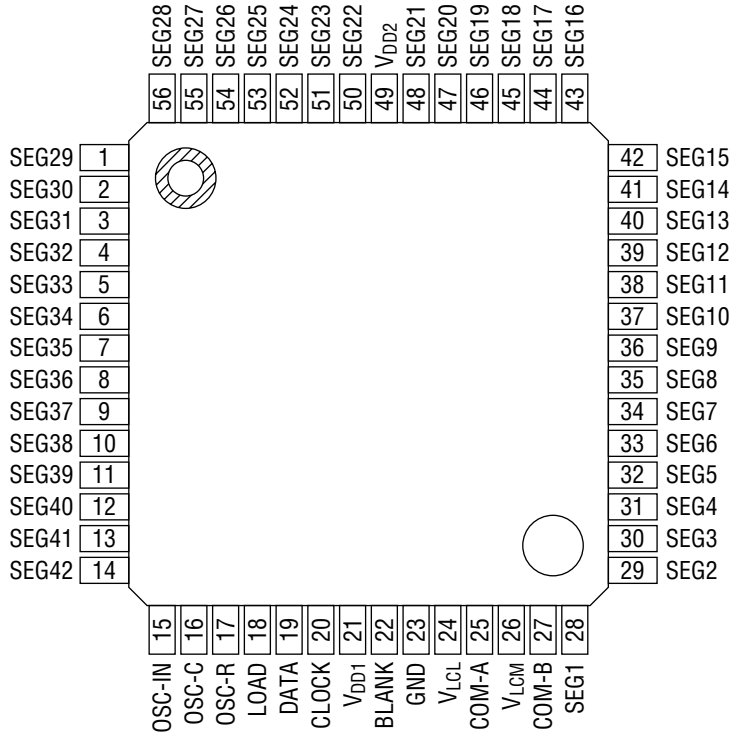
#### FEATURES

- Power supply voltage ( $V_{DD}$ ): 3 to 6V
- LCD driving voltage : 3 to  $V_{DD}$
- Operating temperature :  $-40$  to  $+85^{\circ}\text{C}$
- Applicable LCD panel : 1/2 duty, 84 segments (Max)
- Data transmitting clock : 4 MHz (Max)
- Package:  
56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name : MSM6544GS-2K)

#### BLOCK DIAGRAM



**PIN CONFIGURATION (TOP VIEW)**



**56-Pin Plastic QFP**

## PIN DESCRIPTIONS

- **OSC-IN, OSC-C, OSC-R**  
An RC oscillator circuit for 3-pin type can be configured. Since the OSC-IN pin is in a high input impedance state, it is susceptible to noise.
- **DATA-IN**  
This is the display data input. When this pin is at "H" level, the segments are turned on and when at "L" level, the segments are turned off.
- **CLOCK**  
Pin for clocking display data in. Display data is shifted on the rising edge of the clock pulse.
- **LOAD**  
This is the signal for latching the shift register data. When this pin is set at a "H" level, the shift register data is transmitted to LATCH <A> or LATCH <B>.
- **SEG1 - SEG42**  
These pins drive the LCD segments.
- **COM-A, COM-B**  
These pins drive the LCD commons. COM-A and COM-B correspond to LATCH <A> output and LATCH <B> output, respectively.
- **V<sub>DD2</sub>**  
This is connected to the V<sub>DD1</sub> pin internally.
- **V<sub>LCM</sub>**  
This is the center bias pin of the LCD. Supply the middle voltage between V<sub>DD</sub> and V<sub>LCL</sub>.
- **V<sub>LCL</sub>**  
This is the power supply pin of the LCD driver. The contrast of the LCD can be adjusted by changing the voltage at this pin, but do not set the voltage less than the GND level.
- **BLANK**  
This pin is used to test the all segment outputs (SEG<sub>1</sub> to SEG<sub>42</sub>). All segment outputs are turned off when this pin is set to "H" level. The display returns to the condition before the pin was set to "H" level.
- **V<sub>DD1</sub>, GND**  
These are power supply voltage and ground pins.

**ABSOLUTE MAXIMUM RATINGS**

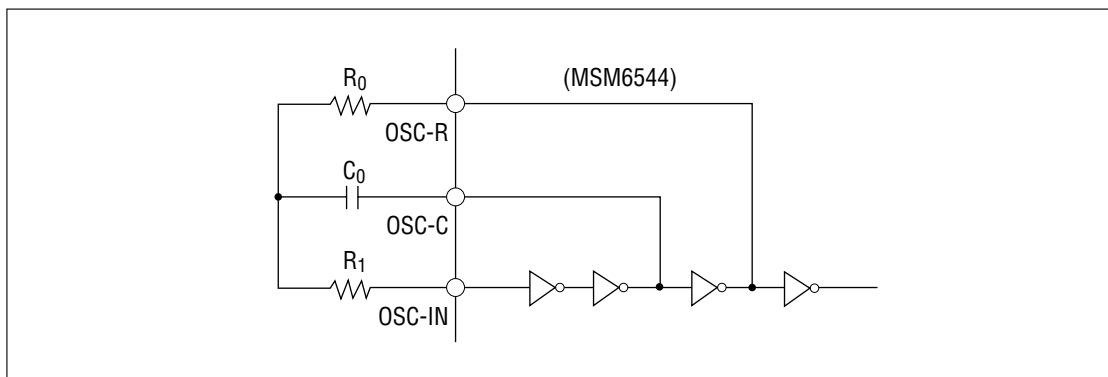
Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{DD}$	$T_a = 25^{\circ}\text{C}$	-0.3 to +6.5	V
Input Voltage	$V_I$	$T_a = 25^{\circ}\text{C}$	GND-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	$^{\circ}\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	$V_{DD}$	—	3 to 6	V
Operating Temperature	$T_{op}$	—	-40 to +85	$^{\circ}\text{C}$
LCD Driving Voltage	$V_{LCD}$	$V_{DD} - V_{LCL}$	3 to $V_{DD}$	V

**OSC Circuit**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Oscillation Resistance	$R_0$	—	10	—	68	$k\Omega$	OSC-R
Oscillation Capacitance	$C_0$	Film capacitor	0.001	—	0.047	$\mu\text{F}$	OSC-C
Current Control Resistance	$R_1$	—	33	—	220	$k\Omega$	OSC-IN
Common Signal Frequency	$f_{COM}$	—	25	—	250	Hz	COM-A COM-B



**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

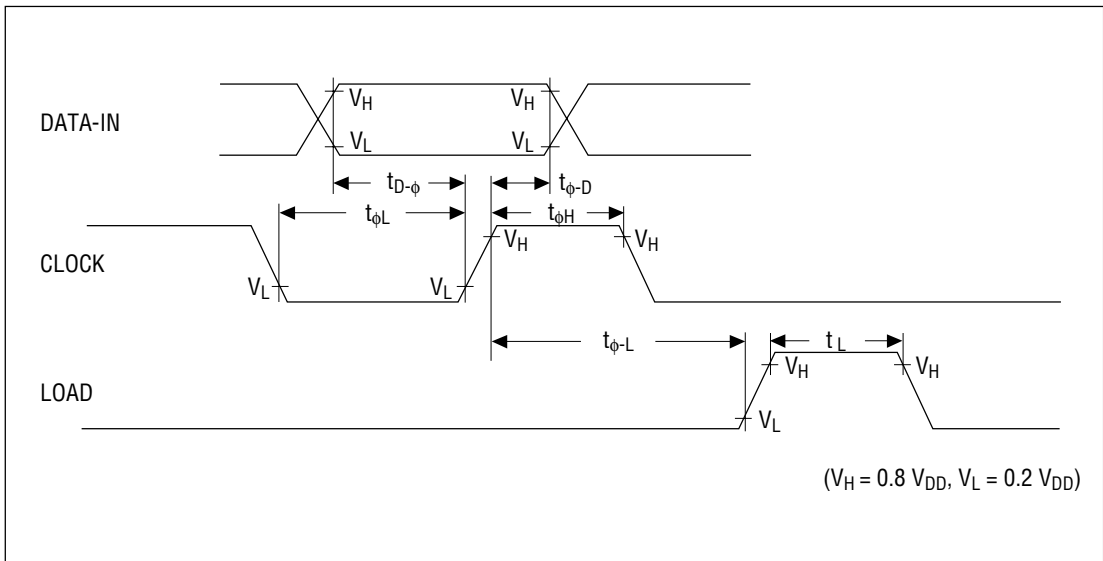
(V<sub>DD</sub> = 5.0V Ta = -40 to +85°C)

Parameter	Symbol	Corresponding Pin	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V <sub>IH</sub>	BLANK LOAD DATA CLOCK OSC-IN	—	3.6	—	V <sub>DD</sub>	V
"L" Input Voltage	V <sub>IL</sub>		—	GND	—	1.0	V
Input Leakage Current	I <sub>LI</sub>		V <sub>I</sub> = 5.0V/0V	—	—	±1	μA
"H" Output Voltage	V <sub>OH</sub>	OSC-R OSC-C	I <sub>O</sub> = -200μA	4.5	—	—	V
		All segment outputs	V <sub>LCM</sub> = 2.5V V <sub>LCL</sub> = 0V I <sub>O</sub> = -30μA	4.8	—	—	V
		COM-A COM-B	V <sub>LCM</sub> = 2.5V V <sub>LCL</sub> = 0V I <sub>O</sub> = -150μA	4.8	—	—	V
"M" Output Voltage	V <sub>OM</sub>	COM-A COM-B	V <sub>LCM</sub> = 2.5V V <sub>LCL</sub> = 0V I <sub>O</sub> = ±150μA	2.3	—	2.7	V
"L" Output Voltage	V <sub>OL</sub>	OSC-R OSC-C	I <sub>O</sub> = 200μA	—	—	0.5	V
		All segment outputs	V <sub>LCM</sub> = 2.5V V <sub>LCL</sub> = 0V I <sub>O</sub> = 30μA	—	—	0.2	V
		COM-A COM-B	V <sub>LCM</sub> = 2.5V V <sub>LCL</sub> = 0V I <sub>O</sub> = 150μA	—	—	0.2	V
Segment Output Impedance	R <sub>SEG</sub>	All segment outputs	V <sub>LCM</sub> = (5+V <sub>LCL</sub> )/2 V <sub>LCL</sub> = 0 to 2V	—	—	10	kΩ
Common Output Impedance	R <sub>COM</sub>	COM-A COM-B	V <sub>LCM</sub> = (5+V <sub>LCL</sub> )/2 V <sub>LCL</sub> = 0 to 2V	—	—	1.5	kΩ
Static Supply Current	I <sub>DD1</sub>	V <sub>DD</sub>	Fix all inputs to V <sub>DD</sub> or GND	—	—	100	μA
Dynamic Supply Current	I <sub>DD2</sub>		No load R <sub>0</sub> = 47kΩ C <sub>0</sub> = 0.0047μF R <sub>1</sub> = 150kΩ	—	0.22	0.5	mA

Switching Characteristics

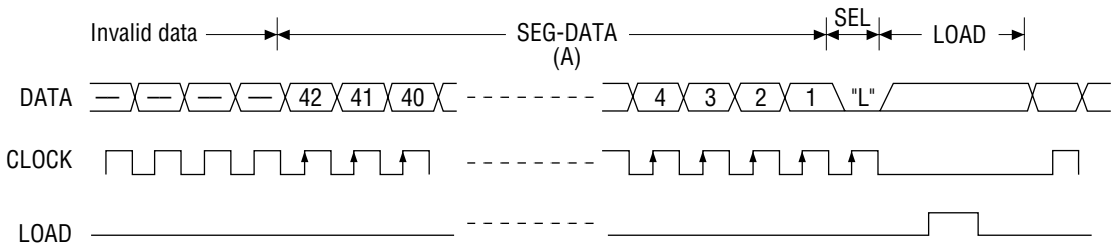
( $V_{DD} = 3.0$  to  $6.0V$ ,  $T_a = -40$  to  $+85^\circ C$ )

Parameter	Symbol	Corresponding Pin	Condition	Min.	Max.	Unit
Clock Pulse Frequency	$f_\phi$	CLOCK	—	—	4	MHz
Clock Pulse "H" Time	$t_{\phi H}$		—	100	—	ns
Clock Pulse "L" Time	$t_{\phi L}$		—	100	—	ns
Data Setup Time	$t_{D-\phi}$	DATA	—	80	—	ns
Data Hold Time	$t_{\phi-D}$	CLOCK	—	40	—	ns
Load Pulse "H" Time	$t_L$	LOAD	—	100	—	ns
Clock-Load Timing	$t_{\phi-L}$	LOAD	—	100	—	ns
OSC-IN Input Frequency	$f_{osc}$	OSC-IN	—	—	20	kHz

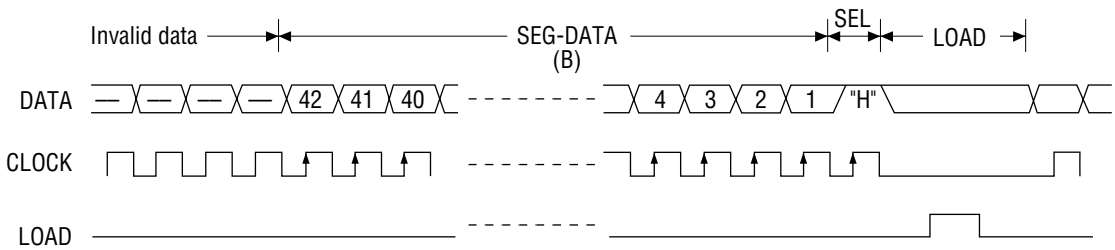


**Data Input Timing**

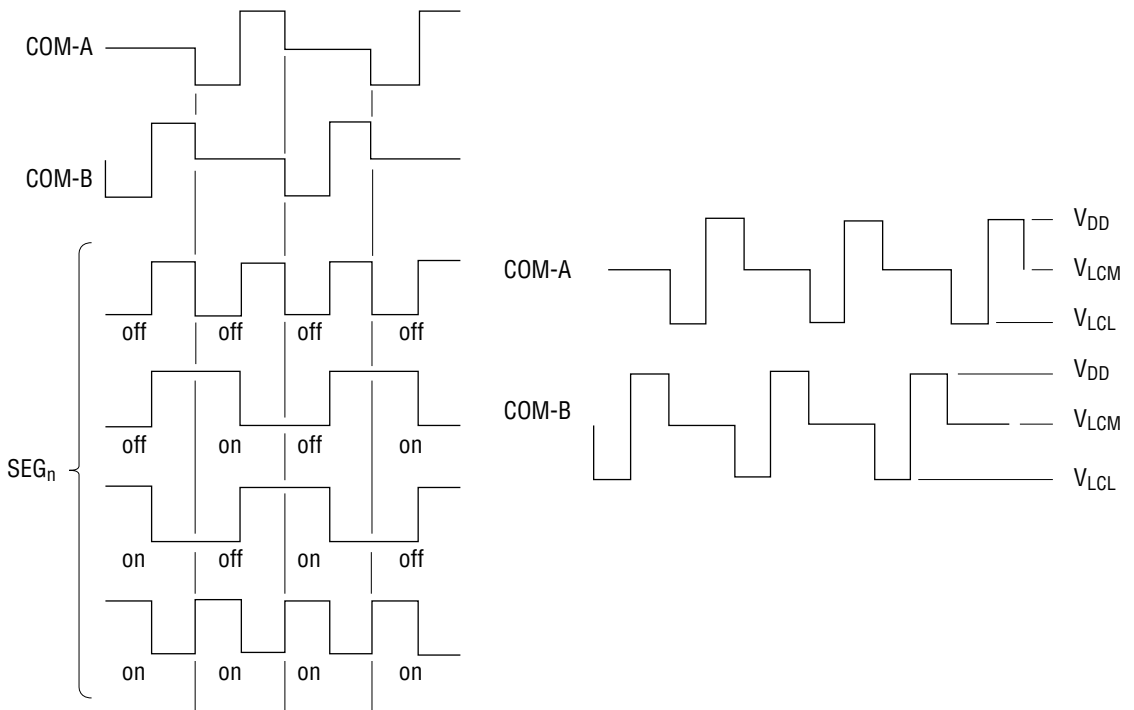
**• DATA input timing for COM-A**



**• DATA input timing for COM-B**



**Output Waveforms**



## FUNCTIONAL DESCRIPTION

### Data Input

The data input consists of the following three timing sections:

- i) SEG-DATA section (42-bit)
- ii) SEL bit section (1-bit)
- iii) LOAD section

A total of 43 bits of 42-bit segment data and 1-bit select bit are taken in the 43-bit shift register at the rising edge of the clock.

The segment data corresponds to "L" (segment OFF) and "H" (segment ON). Input the segment data from SEG42 to SEG1 in this order.

The select bit following the segment data is a bit used to specify the transmit destination of the segment data. The selection is performed as follows.

"L" : LATCH <A> ; corresponds to COM-A

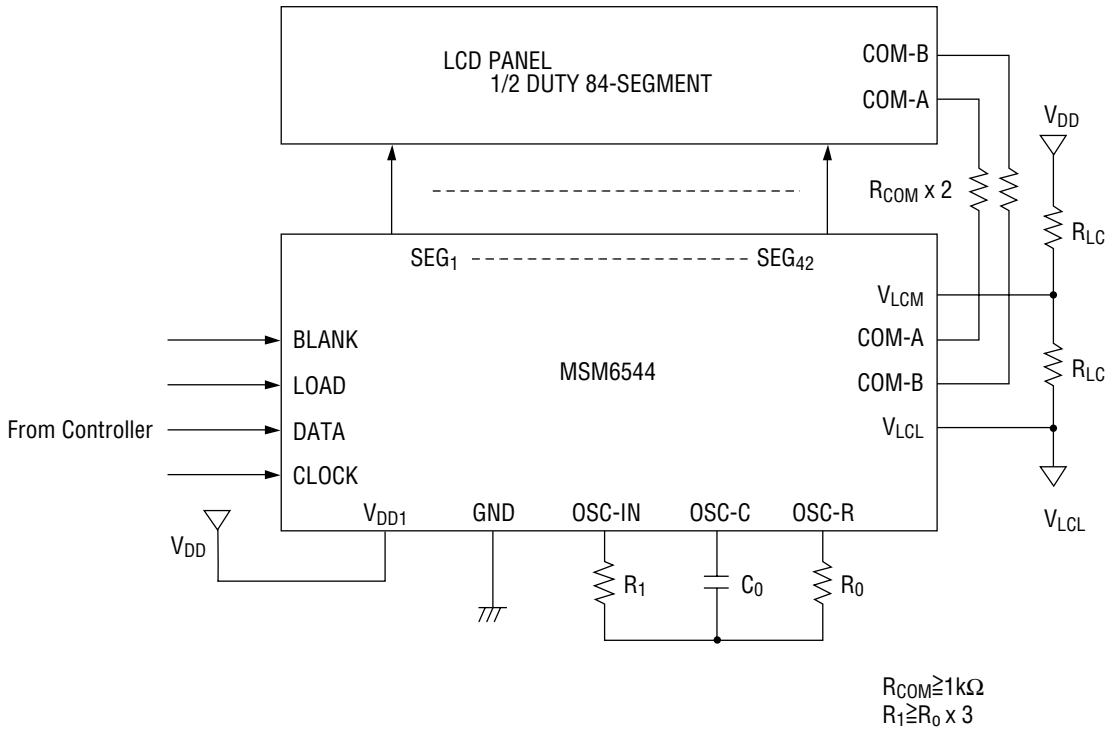
"H" : LATCH <B> ; corresponds to COM-B

The data from the shift register to LATCH <A> or LATCH <B> is transmitted when the LOAD pin is at the "H" level.

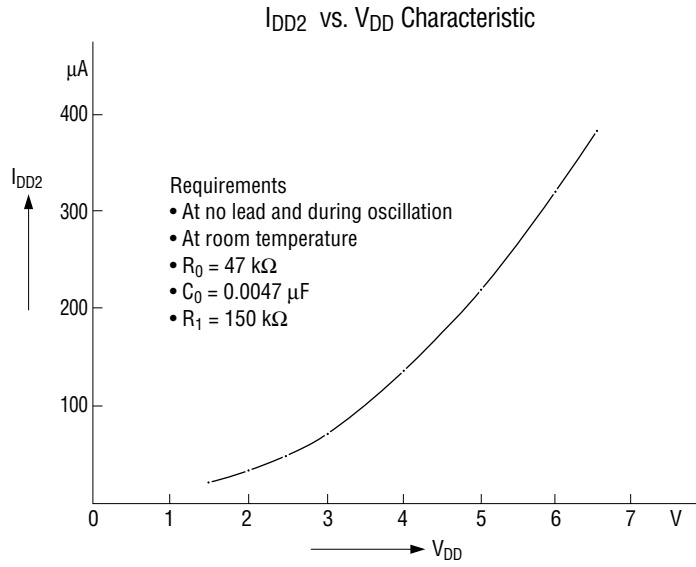
The indication corresponding to the transmit destination latch is also changed at the same time that data is transmitted.



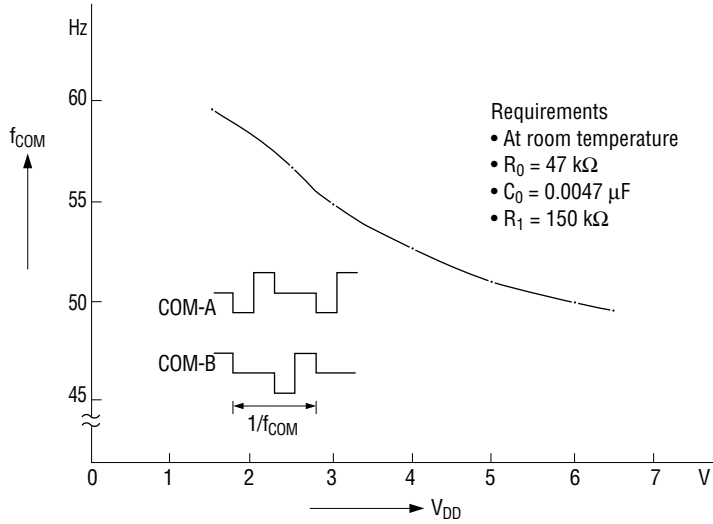
APPLICATION CIRCUITS



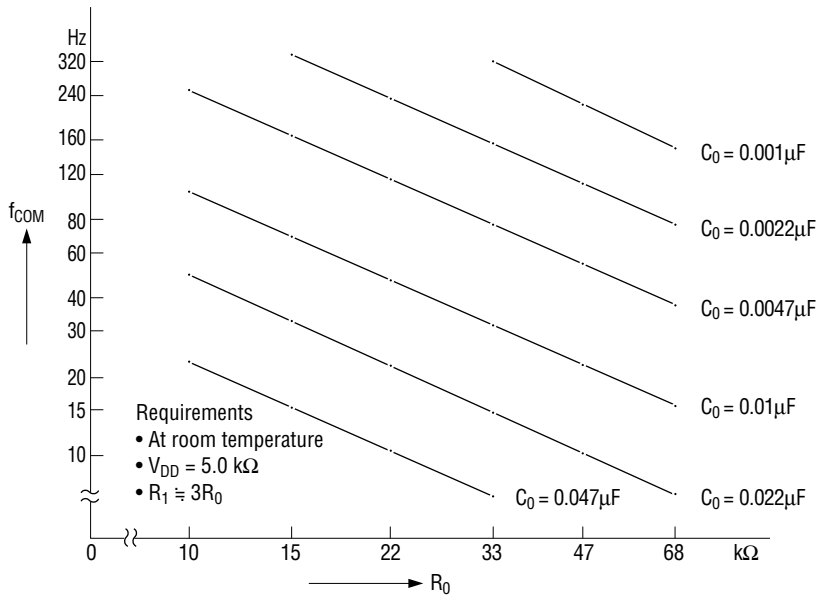
REFERENCE DATA



$f_{COM}$  vs.  $V_{DD}$  Characteristics

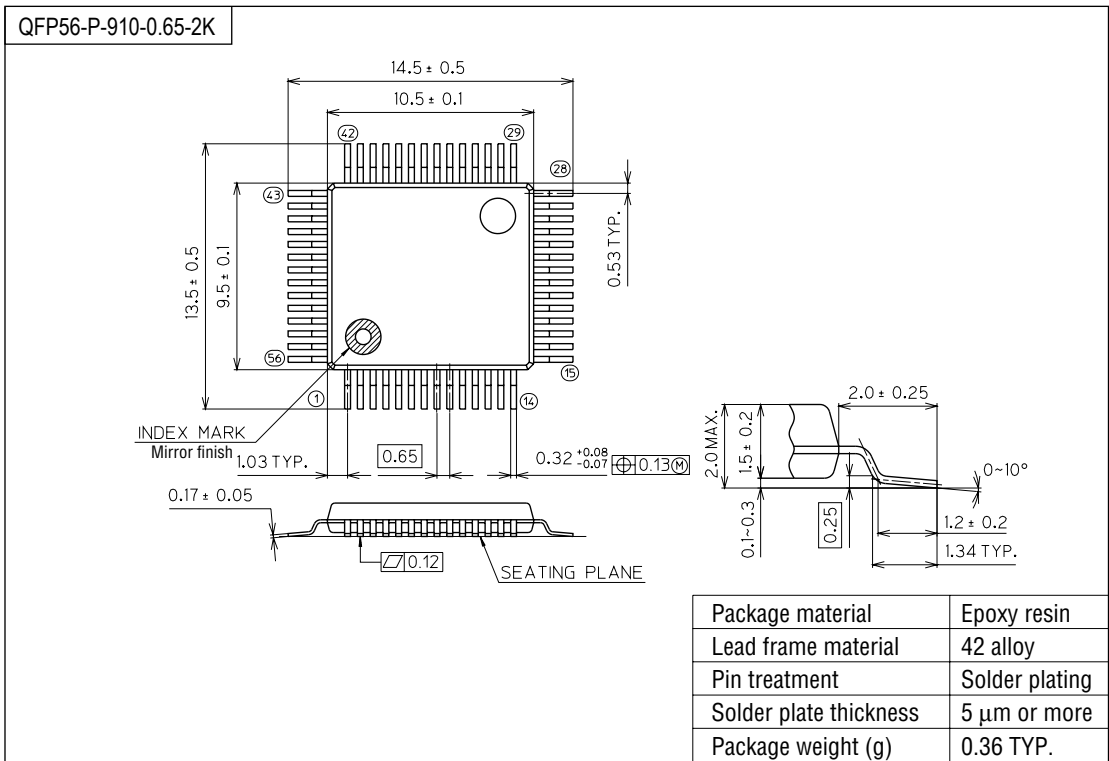


$f_{COM}$  vs.  $R_0$  Characteristics



PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

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